IN THE CLAIMS

Claims 1-10 have previously been canceled without prejudice as being drawn to a non-elected invention.

Please amend claims 11-14 and 16.

Please enter the pending claims as follows:

1. - 10. (Canceled)

11. (Currently Amended) A structure comprising:

an anisotropic conductive film, said anisotropic conductive film comprising multiple layers, said anisotropic conductive film comprising a front surface and a rear surface, said anisotropic conductive film comprising particles of a consistent shape, said particles comprising a non-conductive bulk material, a conductive intermediate layer, and a non-conductive outer layer wherein said non-conductive outer layer may be moved aside by pressure;

a first raised contact disposed over said front surface, said first raised contact forming part of a first wafer; and

a second raised contact disposed over said rear surface, said second raised contact forming part of a second wafer, wherein said second raised contact faces said first raised contact.

- 12. (Currently Amended) The structure of claim 11 wherein said anisotropic conductive film comprises certain particles that are trapped between said first raised contact and said second raised contact, said certain particles that are trapped being deformed by up to about 25-30 % of their nominal diameter.
- 13. (Currently Amended) The structure of claim 12 wherein said particles that are trapped between said first raised contact and said second raised contact form a continuous and conductive path, said continuous and conductive path being zigzagged.
- 14. (Currently Amended) The structure of claim 12 wherein said anisotropic conductive film further comprises other particles that are not trapped between said first raised contact and said second raised contact wherein a ratio of said untrapped particles to said trapped particles may be about 3:1.
- 15. (Original) The structure of claim 13 wherein said particles that are not trapped between said first raised contact and said second raised contact do not form a continuous and conductive path.
- 16. (Currently Amended) A stacked-substrate structure comprising: a first substrate with a first surface, said first surface having a first raised contact;

conductive adhesive having filler including particles with a consistent shape; and

a second substrate with a second surface, said second surface having a second raised contact, said second surface disposed over said anisotropic conductive adhesive, wherein said second raised contact faces said first raised contact, wherein some of said particles are trapped between said second raised contact and said first raised contact to form a continuous and conductive path, and wherein said trapped particles may be locked in a compressed state.

- 17. (Previously Presented) The stacked-substrate structure of claim 16 wherein said first surface is a front surface and said second surface is a front surface.
- 18. (Previously Presented) The stacked-substrate structure of claim 16 wherein said first surface is a front surface and said second surface is a rear surface.
- 19. (Previously Presented) The stacked-substrate structure of claim 16 wherein said first surface is a rear surface and said second surface is a rear surface.
- 20. (Previously Presented) The stacked-substrate structure of claim 16 wherein said first substrate and said second substrate are structurally similar.
- 21. (Previously Presented) The stacked-substrate structure of claim 16 wherein said first substrate and said second substrate are functionally similar.

- 22. (Previously Presented) The stacked-substrate structure of claim 16 wherein said first substrate and said second substrate are structurally and functionally dissimilar.
- 23. (Previously Presented) The stacked-substrate structure of claim 16 wherein said first substrate and said second substrate are pre-thinned.
- 24. (Previously Presented) The stacked-substrate structure of claim 16 wherein said first substrate and said second substrate are wafers.
- 25. (Previously Presented) The stacked-substrate structure of claim 16 wherein said first substrate and said second substrate are portions of wafers.